A 5–11GHz True-Time Delay Utilizing a Pseudo-Time Delay Circuitry in 65nm CMOS

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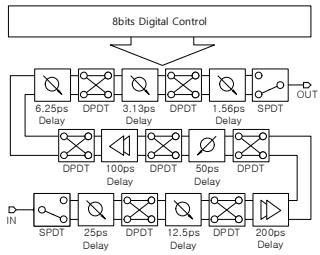
Introduction

❖ A typical true time delay circuit has a group delay error due to the self-resonance frequency of inductor.

➢ We propose double artificial delay line structure to decrease the error



A block diagram of the proposed true time delay circuit

TTD Design

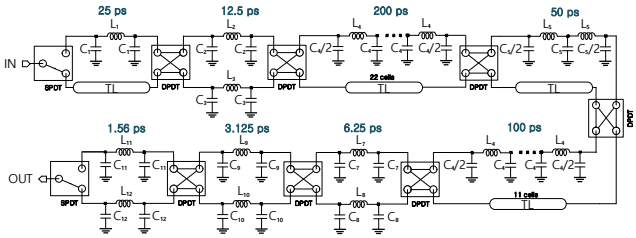


Fig. 1. Schematic of the propose True Time Delay Cirucit.

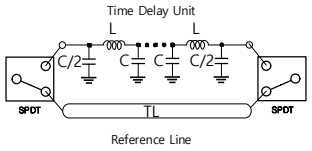


Fig. 2. Schematic of conventional time delay Structure

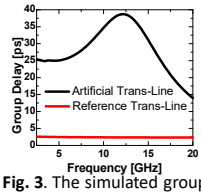


Fig. 3. The simulated group delay error of conventional structure.

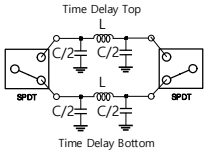


Fig. 4. Schematic of proposed time delay Structure

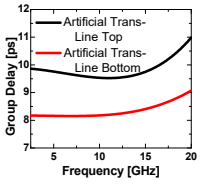


Fig. 5. The simulated group delay error of proposed structure.

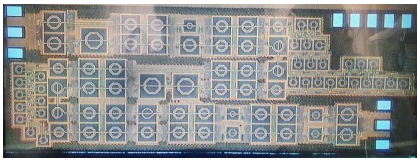


Fig. 6. Chip photo of Proposed time delay structure

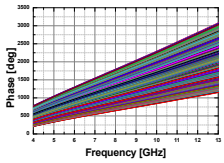


Fig. 7. Simulated phase state of proposed time delay structure

Acknowledgements

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Measurement results

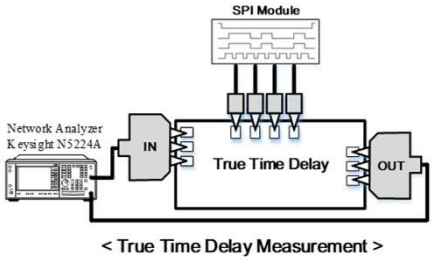

Fig. 6. Measurement setup of True Time Delay Circuit

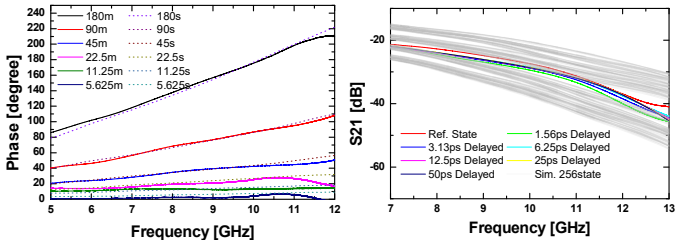

Fig. 7. Measured and Simulated phase state result, S_{21} of Main bit State

Comparison table

Ref.	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[This Work]
Maximum Delay	35.2	400	32.8	42	12.5	106	250	400
f_{RF} [GHz]	20-30	1-20	10-50	15-40	20-40	5-20	6-18	5-11
Chip area [mm²]	0.18 (Core)	4	0.22	0.99	0.1	0.88	2.45	2.91
Resolution	0.56ps	5ps	cont	3ps	cont	3.12ps	1ps	1.54ps
DC power [mW]	-	2.6-6	passive	8.6-24.6	33	passive	passive	passive
Gain [dB]	-	-	±1.3	±2	±1.4	-	-	-
Tech	65nm cmos	130nm cmos	250nm sige	130nm cmos	250nm sige	180nm cmos	180nm cmos	65nm cmos
Structure	TTD (conventional)	TTD (with trombone)	TTD (with varactor lc)	TTD (with trombone)	TTD (with varactor lc,Gm-RC)	TTD (conventional)	TTD (conventional)	TTD
Loss/Delay [dB/ps]	0.35	0.06	0.47	0.36	-	0.19	0.1	0.075

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